

THE COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor: Ryohei Kuki, et al.

For: POST-PROCESSOR USING A NOISE WHITENED MATCHED FILTER FOR A MASS DATA STORAGE DEVICE, OR THE LIKE

Enclosed are:

- ☒ 8 sheets of drawing.
- ☒ An assignment of the invention to Texas Instruments, Inc.
- ☐ A certified copy of a \_\_\_\_\_ application
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☐ Checks in the amount of \$\_\_\_\_\_ and \$\_\_\_\_\_.

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)
FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	29-20 =	* 9
INDEP CLAIMS	3- 3 =	* 0
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENTED		

\*If the difference in Col. 1 is less than zero, enter "0" in Col. 2.

## SMALL ENTITY

RATE	FEE
	\$
x9 =	\$
x39 =	\$
x130 =	\$
TOTAL	\$

OR  
OR  
OR  
OR  
OR  
OROTHER THAN A  
SMALL ENTITY

RATE	FEE
	\$760
x18 =	\$162
x78 =	\$
+260 =	\$
TOTAL	\$922

- ☒ Please charge my Deposit Account No. 20-0668 in the amount of \$922.00 to cover the filing fee. A duplicate copy of this sheet is enclosed.
- ☐ A check in the amount of \$\_\_\_\_\_ to cover the filing fee is enclosed. A check in the amount of \$\_\_\_\_\_ is enclosed for recording assignment.
- ☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 20-0668. A duplicate copy of this sheet is enclosed.
- ☒ Any additional filing fees required under 37 CFR 1.16.
- ☒ Any patent application processing fees under 37 CFR 1.17.
- ☐ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account 20-0668. A duplicate copy of this sheet is enclosed.
- ☐ Any patent application processing fees under 37 CFR 1.17.
- ☐ The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).
- ☐ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

*Richard A. Bachand*  
Richard A. Bachand Reg. No. 25,107  
GROOVER & BACHAND PC  
5353 Wyoming Blvd., NE, Suite 3  
Albuquerque, New Mexico 87109-3132  
Tel: (505) 823-1993

January 13, 1999

Express Mail No. EF537007990US  
Attorney Docket No. TI-28532

01/13/99

jc612 U.S. PTO

jc542 U.S. PTO  
09/229945

01/13/99

POST-PROCESSOR USING A NOISE WHITENED MATCHED FILTER FOR A MASS  
DATA STORAGE DEVICE, OR THE LIKE

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to improvements in mass data storage devices, or the like, and more particularly to improvements in methods and apparatuses for improving data detection in mass data storage devices of the type that use EPR4 Viterbi data detection techniques.

2. RELEVANT BACKGROUND

In the construction of mass data storage devices, or the like, in particular in the construction of the data channel used in digital magnetic recording systems or the like, there has been significant recent interest in Partial Response Maximum-likelihood (PRML) signaling techniques. The most common PRML systems are PR4ML (a partial response class 4) and EPR4ML (extended partial response class 4). Maximum-likelihood detectors, which use a Viterbi algorithm, are generally used for these partial response channels.

In such systems, the use of EPR4 Viterbi data detection techniques is widely used. EPR4 Viterbi detectors are well known, and involve probabilistic techniques for determining data states in the data channel. As data rates increase in the data channel, it becomes increasingly difficult to distinguish adjacent data pulses, and the Viterbi techniques have been found to be very useful.

Unfortunately, significant errors still occur in data detection. For example, using EPR4 techniques, a bit error rate (BER) of about  $10^{-5}$  typically occurs. However it has been observed that if the signal to noise ratio in a system could be reduced by, for example, 1 dB, the bit error rate can be improved to  $10^{-6}$ ,

representing an order of magnitude improvement. Thus, even small improvements in the signal-to-noise ratio results in large improvements in the bit error rate using EPR4 detection techniques. This is significant since presently the requirements exist for the provision of circuits that have a bit error rate less than  $10^{-7}$ , and it is expected that this requirement will continue to become more stringent.

In the past, a typical EPR4 circuit would receive an input signal that has been amplified by a pre-amplifier from the data transducer of the storage device. The amplified signal is applied to an EPR4 equalizer that produces an output that is detected by an EPR4 Viterbi detector. The output from the EPR4 Viterbi detector typically contains the desired data which has been decoded using the above the mentioned probabilistic techniques.

Recently, an EEPR4 channel has been introduced. In comparison to the PR4 partial response target, which is  $(1-D)*(1+D)$ , and the EPR4 partial response target, which is  $(1-D)*(1+D)^2$ , the EEPR4 partial response target is  $(1-D)*(1+D)^3$ , where  $D$  is a delay operator, equal to  $e^{jw\tau}$ , where  $w$  is frequency, and  $\tau$  is delay time.

As the processing level is increased, however, several problems have emerged. For example, the EPR4ML channel is expected to yield better performance than the PR4ML channel for higher recording densities, but the complexity of the Viterbi detector used in an EPR4ML channel increases by more than twice, and the maximum data rate decreases. In order to avoid these drawbacks, several techniques have been proposed.

One such technique, for example, referred to as a "Turbo-PRML" detection technique, uses a PR4 Viterbi detector followed by a post-processor for EPR4 signals. In such post-processor techniques, PR4 equalized samples are applied to a PR4 Viterbi detector that produces a preliminary estimate of the binary input sequence. Then,

preliminary estimate is sensed by the post-processor, which produces a final improved estimate of the binary input sequence, for instance by correcting non-overlapping minimum distance error-events.

5        Since the post-processor can use the same metric as an EPR4 Viterbi detector, the criteria used to correct minimum distance error-events can be the same criteria as those used in an EPR4 Viterbi detector to select survivor paths. The main benefits to such post-processing approaches is that the feedback path  
10 associated with the updating process for the Viterbi detector is limited, allowing for more pipeline and higher channel rates.

Fig. 1 is a block diagram of a post-processor circuit 200 that can be used in conjunction with a mass data storage device, or the like, in accordance with the "Turbo PR4" technique described above.  
15 The circuit 200 receives a read back signal as its input on line 201. The signal may be, for example, the output of a pre-amplifier for the signal detected by the head transducer of an associated mass data storage device, or the like. The input line 201 is connected to the input of the PR4 equalizer circuit 214, which  
20 produces an output on line 212 to a PR4 Viterbi detector 216, after having been digitized and sampled. The recovered data output from the PR4 Viterbi detector 216 is applied to a post-processor circuit 220, and more particularly to a Viterbi error correction circuit 222, which produces an output on line 224.

25        The recovered data output from the PR4 Viterbi detector is also applied to a circuit 226, which has a transfer function equal to  $(1-D)(1+D)^2$ , in order to condition the signal to match the actual sampled partial response target signal applied to the input of the Viterbi 216. The output from the circuit 226 is subtracted  
30 from the actual sampled partial response target, which has been delayed an amount established by a delay circuit 228 to account for the processing delay introduced by the PR4 Viterbi detector 216.

The subtracted signal represents a PR4 error sample, which is applied to a filter 230, which applies a transfer function  $(1 + D)$  to the signal. The output from the filter 230 represents a tentative EPR4 error sample, which is connected on line 231 to the input of a dominant error pattern detection filter circuit 232 that detects a dominant error pattern in the signal being processed. The output from the detection filter 232 is applied to the Viterbi error correction circuit 222 to correct the recovered data signal produced at the output of the Viterbi detector 216 in accordance with the particular error pattern detected by the error pattern detection filter 232. As mentioned, the post-processor 220 can improve the performance of a PR4ML channel to that of an EPR4ML channel.

Another technique that has been used is referred to as simplified partial error response detection (SPERD). A SPERD detector considers only two types of error-events ending at each state along the path of the PR4 Viterbi. Since short error-events are more likely than long error-events, this approach considers only the two shortest Euclidean distance error events, which correspond to making one or two symbol errors. One drawback of this approach is that the probabilities of longer error-events increase in modulation codes with looser constraints. The recent progress of semiconductor process technology can easily realize a full EPR4ML channel IC without any turbo technique mentioned above, but the demand of the higher recording densities will require better performance than an EPR4ML channel.

The performance of the EPR4ML channel would be expected to be improved by an additional EEPR4 post-processor that uses a  $(1+D)$  filter. But in fact such post-processor using a  $(1+D)$  filter and tentative EEPR4 error samples does not actually improve performance, and, moreover, even the performance of an EEPR4 channel is not be improved by a EEEPR4 post-processor which uses a



(1+D) filter and tentative EEP4 error samples. Thus, as the detection circuitry becomes more complex, for example, in circuitry in which the equalizer and Viterbi are EPR4, or EEP4, devices, previously used post-processors can not be used.

5       What is needed, therefore, is a post-processor that can improve the performance of both the EPR4ML and EEP4ML channels.

#### SUMMARY OF THE INVENTION

10       In light of the above, therefore, it is an object of the invention to provide a post-processor that can improve the performance of both the EPR4ML and EEP4ML channels of a mass data storage device, or the like, but which can be applied to other target partial response channels as well.

15       Thus, according to a broad aspect of the invention, a sampled data detection technique is presented for use in a mass data storage device. The technique includes equalizing and sampling a read back signal from a transducer head of the mass data storage device to a partial response level of at least EPR4 to produce an actual sampled partial response target signal. The actual sampled partial response target signal is detected in a Viterbi detector, which having a partial response detection level of at least EPR4 to produce a recovered data output signal. The actual sampled partial response target signal is delayed for a time substantially equal to a time required by the Viterbi detector to generate the recovered data output signal from the actual sampled partial response target signal to produce a delayed actual sampled partial response target signal. The recovered data output signal is converted to a partial response level of the actual sampled data output signal to produce a converted recovered partial response target signal. The converted recovered partial response target signal is subtracted from the delayed actual sampled partial response target signal to produce an error signal. The occurrence of a predetermined error event pattern is determined in the recovered data output signal to produce an

error event pattern indicating signal from which a detection signal is produced having a magnitude based upon the occurrence of an error event. The detection signal is compared to a predetermined threshold level, and an error correction control signal is generated if the data detection signal is larger than the predetermined threshold level, and the error event pattern-indicating signal indicates an occurrence of an error pattern. Finally the recovered data output signal is corrected to correspond to the predetermined data pattern if the error correction control signal has been generated.

The equalizing may include equalizing the read back signal to a partial response level of EPR4 or to EEPR4, and the detecting may include detecting the actual sampled partial response target signal in a Viterbi detector having a partial response detection level of EPR4 or EEPR4.

Determining the occurrence of a predetermined error event pattern in the recovered data output signal comprises determining the occurrence of an error pattern of  $ex = \pm\{1\}$ ,  $ex = \pm\{1-11\}$ ,  $ex = \pm\{1-1\}$ , or other data sequence having a high likelihood of occurrence in the recovered data output signal.

According to another broad aspect of the invention, a post-processor circuit is presented for use in a sampled data read channel of a mass data storage device. The post-processor includes a Viterbi detector that receives an actual sampled partial response target signal from a storage medium of the mass data storage device to produce a recovered data output signal. An error pattern detector generates an error pattern event-indicating signal if a predetermined error event pattern occurs in the sampled partial response target signal. A circuit is provided for generating an error signal based upon a difference between the recovered data output signal and a delayed the actual sampled partial response

target signal. A threshold circuit generates an error correction control signal if a magnitude of the absolute value of the filtered error signal exceeds a predetermined threshold, and an error correction circuit modifies the recovered data output signal when the error correction control signal and the error event pattern indicating occurrence signal are generated.

#### BRIEF DESCRIPTION OF THE DRAWING

The invention is illustrated in the accompanying drawings, in which:

Fig. 1 is a block diagram of a post-processor circuit that can be used in conjunction with a mass data storage device, or the like, in accordance with the prior art.

Fig. 2 is a block diagram of a 16/17 EPR4 detector, which includes a post-processor circuit that can be used in conjunction with a mass data storage device, or the like, in accordance with a preferred embodiment of the invention.

Fig. 3 is a block diagram of a dominant error pattern detector, which may be used in the detector of Fig. 2, in accordance with a preferred embodiment of the invention.

Fig. 4 is a block diagram of a portion of a channel of a mass data storage device, or the like, representing a 16/17 code EPR4 channel through which data can be written to and read from a data media, in accordance with a preferred embodiment of the invention.

Fig. 5 is a box diagram showing an error pattern validation algorithm that can be used to minimize false detection by deciding whether or not an error correction should be made in processed data at an output of a PR4 Viterbi detector, in accordance with a preferred embodiment of the invention.

Fig. 6 is a block diagram error detection filter for a data error pattern of  $ex = \pm\{1-11\}$ , in accordance with a preferred



embodiment of the invention, which may be used in the circuit of Fig. 2.

Fig. 7 is a block diagram error detection filter for a data error pattern of  $ex = \pm\{1\}$ , in accordance with a preferred embodiment of the invention, which may be used in the circuit of Fig. 2.

Fig. 8 shows a graph of a computer simulation comparing the bit error rate performance with and without the post-processor for an EPR4ML channel, in accordance with a preferred embodiment of the invention.

And Fig. 9 is the optimized error pattern detection filters for data error patterns of  $ex = \pm\{1-1\}$  in a Trellis 8/9 code EEPR4 channel, in accordance with a preferred embodiment of the invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A portion of a read channel of a mass data storage device, which includes a 16/17 EPR4 detector, according to a preferred embodiment the invention, is shown in Fig. 2. The detector can be used to determine and correct error patterns in signals that have been equalized by an EPR4 equalizer 12 and detected by an EPR4 Viterbi detector 14, using a post-processing circuit 16. The post-processing circuit 16 receives the recovered data output signal from the EPR4 Viterbi detector 14 and processes it to determine whether an error has occurred with respect to the two data error patterns that are statically most likely to occur, namely  $ex = \pm\{1\}$  and  $ex = \pm\{1-11\}$ .

To make this error pattern determination and correction, the output signal from the EPR4 equalizer 12 is digitized, sampled, and applied to a delay circuit 18 to produce a delayed actual sampled partial response target signal from which the recovered data output from the Viterbi detector 14 is subtracted, after having been

modified by a circuit having a transfer function of  $(1 - D)(1 + D)^2$ . The difference signal on line 22 represents an error signal, which provides an input to a circuit 24 that detects the presence of dominant error patterns.

5        Details of the dominant error pattern detector circuit 24 are described below with respect to Fig. 3. The circuit 24 determines whether one of the dominant error patterns has been miss-detected through threshold-determining techniques described below in detail. When the error pattern detector circuit 24 determines that an error  
10    has occurred in the detection of a dominant data pattern, an output is produced on output line 26 to a circuit 30 which applies a correction to the data pattern.

15        More particularly, the input to the EPR4 Viterbi detector 14 represents the actual sampled value of the EPR4 target. The actual sampled value, of course, includes noise. A perfect signal with no noise present would be represented by  $(1-D)(1+D)^2$ . Consequently, since the output signal from the EPR4 Viterbi detector 14 represents the recovered write current, in order for it to be properly processed, the signal needs to be converted to an EPR4  
20    target signal. Consequently, the transfer function of the block 20 is provided as  $(1-D)(1+D)^2$ .

25        The dominant error pattern detector 24 of Fig. 3 includes a whitening filter 32 followed by an FIR or a matched filter 34. The matched filter 34 may take different forms, depending upon the particular dominant error pattern to be detected. Various circuits that may perform the whitening filter and matched filter function (i.e., the error detection function, are shown in described below with respect to Figs. 6, 7, and 9. In operation, when the error  
30    signal applied to the error detection circuit increases, the signal produced at the output increases. The absolute value of the output is compared to a predetermined threshold, and if it exceeds the threshold, will produce a state change to an AND gate. At the same

time, if the occurrence of a dominant error pattern is detected by a dominant error pattern detector 25, which controls the AND gate of the dominant error pattern detector 24, an output is generated to direct the apply correction circuit 30 to correct the error in the recovered data output from the Viterbi detector 14.

Thus, to summarize the action of the circuit 10, the circuit 10 continually monitors the actual sampled partial response target signal to determine the presence of known error patterns, for example, the two most frequently occurring or dominant error patterns,  $ex = \pm\{1\}$  and  $ex = \pm\{1-11\}$ , with an EPR4 Viterbi detector. Concurrently, the circuit determines an error value on line 35 indicative of the selected dominant error patterns. If the error value on line 35 exceeds a predetermined threshold, the data pattern is corrected.

Fig. 4 is a diagram of a circuit 40 representing a 16/17 code EPR4 channel model. The circuit 40 is intended to write data to or read data from the data medium of a mass data storage device (not shown). To this end, a data media and head transducer are provided, in known manner, as shown in block 42. To write data to the media, the data is first encoded, block 44, for example, with a 16/17 encoding pattern. After encoding, the signal is coded in a pre-code circuit 46 and applied to the head transducer and media 42 by a write driver 48.

On the other hand, to read data previously written to the media of the mass data storage device, the data in its raw form is read from the data media by the head transducer 42 and amplified by a pre-amplifier circuit 50. Typically, the amplitude of the pre-amplified signal is adjusted by a variable gain amplifier (VGA) 52, equalized in an EPR4 equalizer 54, and detected in an EPR4 Viterbi detector 56. A 17/16 decoder 58 then decodes the output from the Viterbi detector 56.

The dominant error patterns of 16/17 code EPR4 channel are shown in Table 1. This table was calculated by assuming that the signal is a Loretzian pulse, the noise is AWGN (Additive White Gaussian Noise), and the equalizer is an ideal filter, which has no equalizer error.

TABLE 1

Error Patterns  ex	Du=2.0			Du=2.75		
	BER			BER		
	$10^{-5}$	$10^{-7}$	$10^{-9}$	$10^{-5}$	$10^{-7}$	$10^{-9}$
$\pm\{1\}$	75.15%	77.98%	79.48%	8.85%	1.83%	.34%
$\pm\{101\}$	.61	.12	.02	.00	.00	.00
$\pm\{10101\}$	.48	.04	.02	.00	.00	.00
$\pm\{1010101\}$	.20	.02	.01	.00	.00	.00
$\pm\{1-11\}$	16.81	16.67	16.22	87.47	97.12	99.35
$\pm\{1-11-11\}$	2.70	2.30	1.91	.94	.26	.06
$\pm\{1-11-11-11\}$	.52	.51	.50	.37	.16	.07
$\pm\{1-11-1\}$	.93	.37	.14	.96	.19	.03
$\pm\{1-11-11-1\}$	1.65	1.61	1.54	.94	.38	.14
$\pm\{1-11-11-11-1\}$	.13	.12	.12	.09	.04	.02
$\pm\{1-1\}$	.69	.14	.03	.37	.02	.00

"Du" means user density which is defined by  $PW50/T_d$ , where PW50 is the pulse width at the 50% amplitude point of the channel step response and  $T_d$  is the duration of the user data bit. The error pattern "ex" is the difference between a correct bit and an error bit at the channel input. "1" means "0" B > "1" error, and "0" means "1" C > "0" error. "0" means no error.

An error pattern "ex" is converted to a 16/17-code error pattern. The converted 16/17 code error patterns of  $ex = \pm\{1\}$  and  $ex = \pm\{1-11\}$  are shown in Table 2.

TABLE 2

ex = $\pm\{1\}$							
		0	1			0	1
		<u>000</u>	$\leftarrow \rightarrow$ <u>101</u>			<u>011</u>	$\leftarrow \rightarrow$ <u>100</u>
		<u>010</u>	$\leftarrow \rightarrow$ <u>111</u>			<u>011</u>	$\leftarrow \rightarrow$ <u>110</u>
ex = $\pm\{1-11\}$							
		0	1			0	1
		<u>01000</u>	$\leftarrow \rightarrow$ <u>10011</u>			<u>00000</u>	$\leftarrow \rightarrow$ <u>11011</u>
		<u>01010</u>	$\leftarrow \rightarrow$ <u>10001</u>			<u>00010</u>	$\leftarrow \rightarrow$ <u>11001</u>
		<u>01001</u>	$\leftarrow \rightarrow$ <u>10010</u>			<u>00001</u>	$\leftarrow \rightarrow$ <u>11010</u>
		<u>01011</u>	$\leftarrow \rightarrow$ <u>10000</u>			<u>00011</u>	$\leftarrow \rightarrow$ <u>11000</u>

The probability of appearance of the error pattern depends on the "Du" and the BER (bit error rate) in code bits. It can be seen from Table I that the two dominant error patterns ("ex" =  $\pm\{1\}$  and "ex" =  $\pm\{1-11\}$ ) occupy more than 90% of all error patterns. Thus, if a post-processor can remove these two dominant error patterns, the BER will be better by more than one order of magnitude.

As indicated above, a post-processor which processes tentative EEPR4 error samples with a (1+D) filter cannot remove most of "ex" =  $\pm\{1-11\}$  error patterns, therefore a performance improvement using this type of filter cannot be expected. The post-processor, therefore, must have better performance than the Viterbi detector for these designated two dominant error patterns.

One of the main reasons that the "ex" =  $\pm\{1\}$  errors and the "ex" =  $\pm\{1-11\}$  errors are dominant is that the noise of these two



patterns is enhanced by the correlation of colored noise in the channel. More particularly, the input noise to the read channel is mainly electronic noise and media noise. The electronic noise is white noise that has constant power in the frequency domain, and does not have any correlation. On the other hand, the media noise is colored noise whose spectrum is not constant, and has correlation. Even if the input noise to read channel is 100% white noise, the equalizer filter colors the noise, which results in the noise having at least some correlation. In fact, the correlated noise often degrades the BER performance of the Viterbi detector (noise correlation loss). The noise correlation loss depends on the error pattern and "Du". The calculated noise correlation loss of an EPR4 Viterbi is shown in Table 3.

TABLE 3

Error Pattern	Du=2.00	Du=2.75
Ex = ±{1}	1.675 dB	1.110 dB
Ex = ±{1-11})	1.630 dB	2.532 dB

Thus, this invention offers a method to implement a post-processor that reduces the noise correlation loss and improves the BER performance. The error pattern detection filter 24 of this invention therefore includes a noise-whitening filter 32 and an error pattern matched filter 34. The noise-whitening filter 32 whitens the noise colored by the equalizer, and the error pattern matched filter 34 is a maximum-likelihood detector for the output signals of the noise whitening filter 32.

The transfer function of the noise-whitening filter 32 is:

$$NW(D) = (1+a_1*D+a_2*D^2+...+a_n*D^n)/(1+b_1*D+b_2*D^2+...+b_m*D^m)$$

where  $a_1, a_2, \dots, a_n$  and  $b_1, b_2, \dots, b_m$  are coefficients that depend upon the recording densities of the data on the media of the mass data storage device. Although the noise is not completely

whitened by this filter, by optimizing the above coefficients the whitening filter can remarkably reduce any noise correlation loss, and can improve the BER performance.

Thus, to analyze the circuit 10, the transfer function of the "ex" =  $\pm\{1-11\}$  data pattern is  $EX(D) = \pm(1-D+D^2)$ .

The transfer function of the ex =  $\pm\{1\}$  data pattern is  $EX(D) = \pm(1)$ .

The transfer function of the EPR4 channel is  $EPR(D) = (1-D)*(1+D)^2$ .

10 The overall transfer function of the output of the noise-whitening filter is  $EY(D) = EX(D)*EPR(D)*NW(D)$ .

The matched filter of the error pattern "ex" =  $\pm\{1-11\}$  is derived by replacing D of EY(D) to  $D^{-1}$ .

$$MF(D) = EY(D^{-1}) = EX(D^{-1})*EPR(D^{-1})*NW(D^{-1}).$$

15 The matched filter MF(D) is a maximum likelihood detector of the error pattern ex =  $\pm\{1-11\}$ .

The transfer function of the error pattern ex =  $\pm\{1-11\}$  detection filter of the post-processor is  $DF(D) = NW(D)*MF(D)$ .

20 For simplicity, the noise-whitening filter can be analyzed using the following transfer function.

$$NW(D) = (1+a1*D+a2*D^2+a3*D^3)/(1+D)$$

The error pattern ex =  $\pm\{1-11\}$  detection filter is

$$DF1(D) = \pm(1+a1*D+a2*D^2+a3*D^3)/(1+D)*(1-D^{-1}+D^{-2})*(1-D^{-1})*(1+D^{-1})^2*(1+a1*D^{-1}+a2*D^{-2}+a3*D^{-3})/(1+D^{-1})$$

$$25 = \pm(c0*(D^3-1)+c1*(D^3-D)+c2*(D^7-D^2)+c3*(D^6-D^3)-c4*(D^6-D^4))$$

where  $c0=a3$ ,

$$c1=a2-2*a3+a1*a3,$$

$$c2=a1-2*a2+a1*a2+2*a3-2*a1*a3+a2*a3,$$

$$c3=1-2*a1+2*a2-a3-2*a1*a2+2*a1*a3-2*a2*a3+a1^2+a2^2+a3^2$$

$$30 c4=2-3*a1+a2-3*a1*a2+a1*a3-3*a2*a3+2*a1^2+2*a2^2+2*a3^2$$

Using a similar method, the error pattern an "ex" =  $\pm\{1\}$  detection filter is:

$$DF2(D) = \pm(c8*(D^7-1)+c5*(D^6-D)+c6*(D^5-D^2)+c7*(D^4-D^5))$$

5 The optimization of the coefficients of the error pattern detection filters is done by maximizing the SNR of the output of the error pattern detection filters by computer techniques. The signal of the error pattern detection filter is equal to the squared Euclidean distance of the EY(D).

For "ex" =  $\pm\{1-11\}$ ,  $S\{1-11\} = 2*(c2 + c4)$ .

10 For "ex" =  $\pm\{1\}$ ,  $S(1) = 2*(c6 + c7)$ .

The optimum detection threshold voltage of the error pattern detection filter is a half of  $S\{1-11\}$  and  $S\{1\}$ .

Therefore,  $V_{thA} = c2 + c4$  for "ex" =  $\pm\{1-11\}$ .

And  $V_{thB} = c6 + c7$  for "ex" =  $\pm\{1\}$ .

15 If the output signals of the error pattern detection filters are larger than  $V_{thA}$  or  $V_{thB}$ , the error pattern detection filter detects the Viterbi detector error of the error pattern.

The noise spectrum of the output of the error pattern detection filter is:

20 
$$N(w) = N0 * EQ(D) * DF(D).$$

Or 
$$N(w) = N0 * EQ(D) * DF2(D).$$

Where  $EQ(D)$  is the transfer function of EPR4 equalizer filter, and  $N0$  is noise spectrum of the channel input. ( $N0$  is constant for AWGN.)

25 If the ideal equalizer filter and Loretzian pulse is assumed,  $EQ(D) = 2/\pi/k * e^{(w*Ts*k/2)} * (1+D)^2$ .

Where  $Ts$  is a sampling time(equal to  $16/17*Td$ ) and

$$K = PW50/Ts = 17/16*Du.$$

30 The noise power of the output of the error pattern detection filter is:

$$N = \frac{1}{2 * \pi} \int_0^{\pi} |N(w)|^2 dw$$

The optimum coefficients (c0 - c8) and the detection threshold  $V_{thA}$  and  $V_{thB}$  of the error pattern detection filters that maximize the signal to noise ratio can be obtained from the above equations, for example, by computer optimization techniques. (It should be noted that the optimum values of the coefficients and the thresholds depend on the user density,  $D_u$ , because  $EQ(D)$  depends on  $D_u$ .) The error detection filters sometimes have false detection. In order to minimize any such false detection, the validation logic can be employed to decide whether the correction should be done.

Fig. 5 is the error pattern validation algorithm. The precise form of the error pattern validation algorithm depends upon the particular error event that is to be detected and corrected. Thus, for example, for an error event A in which "ex" = {1} or "ex" = {-1} is to be verified, if the detection signal  $f_A$  is  $> V_{thA}$  and  $\hat{C} = \{0\}$ , a correction should be applied. Additionally, if the detection signal  $f_A$  is  $< -V_{thA}$  and  $\hat{C} = \{1\}$ , a correction also should be applied.

On the other hand, if the error event is one in which the signal "ex" = {1,-1,1} or "ex" = {-1,1,-1} is to be validated, if the detection signal  $f_B$  is  $> V_{thB}$  and  $\hat{C} = \{0,1,0\}$ , then a correction occurs. Alternatively, if the detection signal  $f_B$  is  $< -V_{thB}$ , and  $\hat{C} = \{1,0,1\}$ , then the correction the is applied.

It is difficult to avoid incorrect correction completely, and if the value of  $V_{th}$  is slightly increased, the probability of the wrong correction decreases; however, the undetected probability of the Viterbi detector error increases. Computer simulations can obtain the optimum threshold values that minimize the bit error rate of the overall channel.

One embodiment for a dominant error pattern detection filter 32, which can be used to provide the dominant error pattern of "ex" =  $\pm\{1-11\}$ , described above with respect to Figs 2 and 3, is shown in Fig. 6. The detection filter 32 includes 9 delay elements 60 -- 68, each delaying the error signal on error signal input line 31 by one delay unit, D, described above. Outputs from respective delay elements 64 -- 68 are respectively summed with the output from delay blocks 63 -- 60 and the signal on the input line 31. It is noted that in the output of delay block 64 is subtracted from the output of delay block 63, whereas the input signal on line 31 and the outputs from the respective blocks 60 -- 62 are subtracted from the outputs of respective delay blocks 68 -- 65.

The difference signals are weighted by respective weights  $c_0$ ,  $c_1$ ,  $c_2$ ,  $c_3$ , and  $c_4$ , and the weighted signals summed by a summer circuit 70. The output from the summer circuit 70 is a function  $f_A$  expressed by  $f_A = C_0(D^9 - 1) + C_1(D^8 - D) + C_2(D^7 - D^2) + C_3(D^6 - D^3) - C_4(D^5 - D^4)$ . The absolute value of the detection filter output function is taken by absolute value circuit 72 to produce an input to a comparator 74. The magnitude of the input to the comparator 74 is compared to a threshold voltage,  $V_{thA}$ , to produce an output on line 76 from the detector filter circuit 32.

One embodiment for a dominant error pattern detection filter 32 which can be used to detect the "ex" =  $\pm\{1-1\}$ , which can be used to provide dominant error pattern detection in the circuit of Figs. 2 and 3, is shown in Fig. 7. The detection filter 32 includes seven delay elements 80 -- 86, each delaying the error signal on error signal input line 31 by one delay unit, D, described above. The signals on the input lines and respective delay elements 80 -- 82 are respectively subtracted from the outputs from respective delay blocks 86 -- 83.



The difference signals are weighted by respective weights  $c_8$ ,  $c_5$ ,  $c_6$ , and  $c_7$ , and the weighted signals are summed by a summer circuit 90. The output from the summer circuit 90 is a function  $fB$ , which equals  $C_8(D^7 - 1) + C_5(D^6 - D) + C_6(D^5 - D^2) + C_7(D^7 - D^3)$ . The absolute value of the function  $fB$  is produced by absolute value circuit 92 to produce an input to a comparator 94. The magnitude of the input to the comparator 94 is compared to a threshold voltage  $V_{thB}$  to produce an output on line 96 from the detector filter circuit 32.

Thus, using either, or both, of the circuits 32 of Figs. 6 and 7, the post-processor has the selectable two coefficients set. Table 5 is the two sets of coefficients, optimized by computer simulation. The one is for low user density and the other is for high user density.

TABLE 5

	Event B detector					Event A Detector			
	C0	C1	C2	C3	C4	C5	C6	C7	C8
Low User Density (2.0-2.5)	0.25	0.75	0.50	1.00	1.50	0.50	1.00	1.00	0.25
High User Density (2.5-3.0)	0.50	1.00	1.00	1.00	1.00	0.50	1.00	1.00	0.25

Fig. 8 shows the bit error rate performance comparisons by computer simulations with and without the post-processor for an EPR4ML channel. It can be seen that the bits error rate with the post-processor is significantly reduced then without the post-processor, for the same signal to noise ratio.

A noise whitening filter  $NW(D)$  and an error pattern matched filter  $MF(D)$  can be combined into a simple error pattern detection filter  $DF(D)$ . The appropriate selection of  $b_1$ ,  $b_2$  . . . and,  $m$  of the denominator of the equation for  $MW(D)$  above can simplify the equation.

An example of another application of this invention is done for a Trellis 8/9-code EPR4ML channel. This code was proposed by

W. Bliss, "An 8/9 Rate Time-Varying Trellis Code for High Density Magnetic Recording", Intermag 97. A similar code was proposed by P.H. Siegel et al in May 14, 1997 as "Rate 8/9 Trellis Code for E2PR4". This channel is better performance than 16/17 code EPR4 channel for AWGN.

The three dominant error patterns of the Trellis 8/9 code EEPR4ML channel are shown in Table 6.

TABLE 6

Error pattern	Du=2 (SNR=19dB)	Du=3 (SNR=21.5dB)
Ex = $\pm\{1\}$	90.5%	30.8%
Ex = $\pm\{1-1\}$	7.5%	54.9%
Ex = $\pm\{1001\}$	1.1%	11.6%

The structure of the noise-whitening filter of the three dominant error pattern is as follows.

For ex =  $\pm\{1\}$ :  $NW1(D) = (1+a1*D+a2*D^2+3*D^5)/(1+D)$ .

For ex =  $\pm\{1-1\}$ :  $NW2(D) = (1+a1*D+a2*D^2+a3*D^3)/(1+2*D+D^2)$

The selection of this structure simplifies the dominant error pattern detection filters.

The transfer function of ex =  $\pm\{1\}$  is

$DF1(D) = \{c1*(1+D^6)+c2*(D+D^5)+c3*(D^2+D^4)+c4*D^3\}*(1-D^2)$ .

The transfer function of ex =  $\pm\{1-1\}$  is

$DF2(D) = (c5*(1+D^6)+c6*(D+D^5)+c7*(D^2+D^4)+c8*D^8)*(1+D)$ .

The transfer function of ex =  $\pm\{1001\}$  is

$DF3(D) = \{c9*(1+D^6)+c10*(D+D^5)+c11*(D^2+D^4)+c12*D^3\}*(1-D)*(1-D+D^2)$ .

For simplicity, the DF3(D) filter can be removed, at the cost of a small degradation of the high user density performance (0.3dB loss at Du =3, compared with three error pattern detection post-processor). Fig. 9 is the optimized error pattern detection filters of Trellis 8/9 code EEPR4 channel. The EPR4 error signal

detector 32 includes six delay blocks 100 -- 105. The outputs from blocks 105 -- 103 are added respectively to the signals on the input line 31 and the outputs from blocks 100 -- 101. The signals on the input line 31 and outputs from blocks 100 -- 102 are weighted, as shown, by weighting factors  $c_1$ ,  $c_2$ ,  $c_3$ , and  $c_4$  to be summed in a summer 108. In addition, the outputs from blocks 100 and 101 are weighted by weighting factors  $c_5$  and  $c_6$ . The signals weighted by  $c_1$  and  $c_6$  are summed in a second summer 110, and the signals weighted by  $c_4$  and  $c_5$  are subtracted in the summer 110, as shown.

The output from the summer 108 is subtracted from itself after being twice delayed by delay blocks 112 and 114, to produce an output function signal on line 116 to correct for the error event A, or  $\pm\{1\}$ . Similarly, the output from the summer 110 is added to itself after a single delay added by block 120 to produce the error correction function on output line 122 represented by the error event pattern B, or  $\pm\{1-1\}$ .

The performance improvement is about 0.5-0.7 dB in the  $D_u = 2.25-3.25$  for AWGN.

In this case, the coefficients set of these filters is not changed over the above  $D_u$  range.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

I CLAIM:

1 1. A post-processing method for use in a sampled data read channel  
2 of a mass data storage device that has a Viterbi detector that  
3 receives actual sampled partial response target data from a said  
4 data medium of a mass data storage device and produces a recovered  
5 data output signal, comprising:

6 filtering an a recovered partial response target signal  
7 derived from said recovered data output signal and said sampled  
8 partial response target data to produce a filtered output signal;

9 providing a threshold circuit to provide a threshold against  
10 which said filtered output signal is compared;

11 generating an error event pattern indicating signal when a  
12 predetermined error event pattern occurs in said recovered data  
13 output signal;

14 and modifying the recovered data output signal when said  
15 filtered output signal exceeds the threshold of said threshold  
16 circuit and said error event indicating signal is generated.

1 2. The method of claim 1 wherein said Viterbi detector is an EPR4  
2 Viterbi detector.

1 3. The method of claim 1 wherein said Viterbi detector is an EEPR4  
2 Viterbi detector.

1 4. The method of claim 1 wherein said error event pattern is  $ex =$   
2  $\pm\{1\}$ .

1 5. The method of claim 1 wherein said error event pattern is  $ex =$   
2  $\pm\{1-11\}$ .

1 6. The method of claim 1 wherein said error event pattern is  $\text{ex} =$   
2  $\pm\{1-1\}$ .

1 7. The method of claim 1 wherein said filtering is accomplished by  
2 applying said output to an FIR filter.

1 8. The method of claim 1 further comprising whitening the recovered  
2 data output signal, prior to said filtering, with a whitening  
3 filter.

1 9. A sampled data detection technique for use in a mass data  
2 storage device, comprising:

3 equalizing and sampling a read back signal from a transducer  
4 head of said mass data storage device to a partial response level  
5 of at least EPR4 to produce an actual sampled partial response  
6 target signal;

7 detecting said actual sampled partial response target signal  
8 in a Viterbi detector having a partial response detection level of  
9 at least EPR4 to produce a recovered data output signal;

10 delaying said actual sampled partial response target signal  
11 for a time substantially equal to a time required by said Viterbi  
12 detector to generate said recovered data output signal from said  
13 actual sampled partial response target signal to produce a delayed  
14 actual sampled partial response target signal;

15 converting said recovered data output signal to a partial  
16 response level of said actual sampled data output signal to produce  
17 a converted recovered partial response target signal;

18 subtracting said converted recovered partial response target  
19 signal from said delayed actual sampled partial response target  
20 signal to produce an error signal;



21 determining the occurrence of a predetermined error event  
22 pattern in said recovered data output signal to produce an error  
23 event pattern indicating signal;

24 producing, from said error signal, a detection signal having  
25 a magnitude based upon the occurrence of an error event;

26 comparing said detection signal to a predetermined threshold  
27 level, and generating an error correction control signal if said  
28 data detection signal is larger than said predetermined threshold  
29 level, and said error event pattern indicating signal indicates an  
30 occurrence of an error pattern; and

31 correcting said recovered data output signal to correspond to  
32 said predetermined data pattern if said error correction control  
33 signal has been generated.

10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100  
101  
102  
103  
104  
105  
106  
107  
108  
109  
110  
111  
112  
113  
114  
115  
116  
117  
118  
119  
120  
121  
122  
123  
124  
125  
126  
127  
128  
129  
130  
131  
132  
133  
134  
135  
136  
137  
138  
139  
140  
141  
142  
143  
144  
145  
146  
147  
148  
149  
150  
151  
152  
153  
154  
155  
156  
157  
158  
159  
160  
161  
162  
163  
164  
165  
166  
167  
168  
169  
170  
171  
172  
173  
174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193  
194  
195  
196  
197  
198  
199  
200  
201  
202  
203  
204  
205  
206  
207  
208  
209  
210  
211  
212  
213  
214  
215  
216  
217  
218  
219  
220  
221  
222  
223  
224  
225  
226  
227  
228  
229  
230  
231  
232  
233  
234  
235  
236  
237  
238  
239  
240  
241  
242  
243  
244  
245  
246  
247  
248  
249  
250  
251  
252  
253  
254  
255  
256  
257  
258  
259  
260  
261  
262  
263  
264  
265  
266  
267  
268  
269  
270  
271  
272  
273  
274  
275  
276  
277  
278  
279  
280  
281  
282  
283  
284  
285  
286  
287  
288  
289  
290  
291  
292  
293  
294  
295  
296  
297  
298  
299  
300  
301  
302  
303  
304  
305  
306  
307  
308  
309  
310  
311  
312  
313  
314  
315  
316  
317  
318  
319  
320  
321  
322  
323  
324  
325  
326  
327  
328  
329  
330  
331  
332  
333  
334  
335  
336  
337  
338  
339  
340  
341  
342  
343  
344  
345  
346  
347  
348  
349  
350  
351  
352  
353  
354  
355  
356  
357  
358  
359  
360  
361  
362  
363  
364  
365  
366  
367  
368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378  
379  
380  
381  
382  
383  
384  
385  
386  
387  
388  
389  
390  
391  
392  
393  
394  
395  
396  
397  
398  
399  
400  
401  
402  
403  
404  
405  
406  
407  
408  
409  
410  
411  
412  
413  
414  
415  
416  
417  
418  
419  
420  
421  
422  
423  
424  
425  
426  
427  
428  
429  
430  
431  
432  
433  
434  
435  
436  
437  
438  
439  
440  
441  
442  
443  
444  
445  
446  
447  
448  
449  
450  
451  
452  
453  
454  
455  
456  
457  
458  
459  
460  
461  
462  
463  
464  
465  
466  
467  
468  
469  
470  
471  
472  
473  
474  
475  
476  
477  
478  
479  
480  
481  
482  
483  
484  
485  
486  
487  
488  
489  
490  
491  
492  
493  
494  
495  
496  
497  
498  
499  
500  
501  
502  
503  
504  
505  
506  
507  
508  
509  
510  
511  
512  
513  
514  
515  
516  
517  
518  
519  
520  
521  
522  
523  
524  
525  
526  
527  
528  
529  
530  
531  
532  
533  
534  
535  
536  
537  
538  
539  
540  
541  
542  
543  
544  
545  
546  
547  
548  
549  
550  
551  
552  
553  
554  
555  
556  
557  
558  
559  
560  
561  
562  
563  
564  
565  
566  
567  
568  
569  
570  
571  
572  
573  
574  
575  
576  
577  
578  
579  
580  
581  
582  
583  
584  
585  
586  
587  
588  
589  
590  
591  
592  
593  
594  
595  
596  
597  
598  
599  
600  
601  
602  
603  
604  
605  
606  
607  
608  
609  
610  
611  
612  
613  
614  
615  
616  
617  
618  
619  
620  
621  
622  
623  
624  
625  
626  
627  
628  
629  
630  
631  
632  
633  
634  
635  
636  
637  
638  
639  
640  
641  
642  
643  
644  
645  
646  
647  
648  
649  
650  
651  
652  
653  
654  
655  
656  
657  
658  
659  
660  
661  
662  
663  
664  
665  
666  
667  
668  
669  
670  
671  
672  
673  
674  
675  
676  
677  
678  
679  
680  
681  
682  
683  
684  
685  
686  
687  
688  
689  
690  
691  
692  
693  
694  
695  
696  
697  
698  
699  
700  
701  
702  
703  
704  
705  
706  
707  
708  
709  
710  
711  
712  
713  
714  
715  
716  
717  
718  
719  
720  
721  
722  
723  
724  
725  
726  
727  
728  
729  
730  
731  
732  
733  
734  
735  
736  
737  
738  
739  
740  
741  
742  
743  
744  
745  
746  
747  
748  
749  
750  
751  
752  
753  
754  
755  
756  
757  
758  
759  
760  
761  
762  
763  
764  
765  
766  
767  
768  
769  
770  
771  
772  
773  
774  
775  
776  
777  
778  
779  
780  
781  
782  
783  
784  
785  
786  
787  
788  
789  
790  
791  
792  
793  
794  
795  
796  
797  
798  
799  
800  
801  
802  
803  
804  
805  
806  
807  
808  
809  
810  
811  
812  
813  
814  
815  
816  
817  
818  
819  
820  
821  
822  
823  
824  
825  
826  
827  
828  
829  
830  
831  
832  
833  
834  
835  
836  
837  
838  
839  
840  
841  
842  
843  
844  
845  
846  
847  
848  
849  
850  
851  
852  
853  
854  
855  
856  
857  
858  
859  
860  
861  
862  
863  
864  
865  
866  
867  
868  
869  
870  
871  
872  
873  
874  
875  
876  
877  
878  
879  
880  
881  
882  
883  
884  
885  
886  
887  
888  
889  
890  
891  
892  
893  
894  
895  
896  
897  
898  
899  
900  
901  
902  
903  
904  
905  
906  
907  
908  
909  
910  
911  
912  
913  
914  
915  
916  
917  
918  
919  
920  
921  
922  
923  
924  
925  
926  
927  
928  
929  
930  
931  
932  
933  
934  
935  
936  
937  
938  
939  
940  
941  
942  
943  
944  
945  
946  
947  
948  
949  
950  
951  
952  
953  
954  
955  
956  
957  
958  
959  
960  
961  
962  
963  
964  
965  
966  
967  
968  
969  
970  
971  
972  
973  
974  
975  
976  
977  
978  
979  
980  
981  
982  
983  
984  
985  
986  
987  
988  
989  
990  
991  
992  
993  
994  
995  
996  
997  
998  
999  
1000  
1001  
1002  
1003  
1004  
1005  
1006  
1007  
1008  
1009  
1010  
1011  
1012  
1013  
1014  
1015  
1016  
1017  
1018  
1019  
1020  
1021  
1022  
1023  
1024  
1025  
1026  
1027  
1028  
1029  
1030  
1031  
1032  
1033  
1034  
1035  
1036  
1037  
1038  
1039  
1040  
1041  
1042  
1043  
1044  
1045  
1046  
1047  
1048  
1049  
1050  
1051  
1052  
1053  
1054  
1055  
1056  
1057  
1058  
1059  
1060  
1061  
1062  
1063  
1064  
1065  
1066  
1067  
1068  
1069  
1070  
1071  
1072  
1073  
1074  
1075  
1076  
1077  
1078  
1079  
1080  
1081  
1082  
1083  
1084  
1085  
1086  
1087  
1088  
1089  
1090  
1091  
1092  
1093  
1094  
1095  
1096  
1097  
1098  
1099  
1100  
1101  
1102  
1103  
1104  
1105  
1106  
1107  
1108  
1109  
1110  
1111  
1112  
1113  
1114  
1115  
1116  
1117  
1118  
1119  
1120  
1121  
1122  
1123  
1124  
1125  
1126  
1127  
1128  
1129  
1130  
1131  
1132  
1133  
1134  
1135  
1136  
1137  
1138  
1139  
1140  
1141  
1142  
1143  
1144  
1145  
1146  
1147  
1148  
1149  
1150  
1151  
1152  
1153  
1154  
1155  
1156  
1157  
1158  
1159  
1160  
1161  
1162  
1163  
1164  
1165  
1166  
1167  
1168  
1169  
1170  
1171  
1172  
1173  
1174  
1175  
1176  
1177  
1178  
1179  
1180  
1181  
1182  
1183  
1184  
1185  
1186  
1187  
1188  
1189  
1190  
1191  
1192  
1193  
1194  
1195  
1196  
1197  
1198  
1199  
1200  
1201  
1202  
1203  
1204  
1205  
1206  
1207  
1208  
1209  
1210  
1211  
1212  
1213  
1214  
1215  
1216  
1217  
1218  
1219  
1220  
1221  
1222  
1223  
1224  
1225  
1226  
1227  
1228  
1229  
1230  
1231  
1232  
1233  
1234  
1235  
1236  
1237  
1238  
1239  
1240  
1241  
1242  
1243  
1244  
1245  
1246  
1247  
1248  
1249  
1250  
1251  
1252  
1253  
1254  
1255  
1256  
1257  
1258  
1259  
1260  
1261  
1262  
1263  
1264  
1265  
1266  
1267  
1268  
1269  
1270  
1271  
1272  
1273  
1274  
1275  
1276  
1277  
1278  
1279  
1280  
1281  
1282  
1283  
1284  
1285  
1286  
1287  
1288  
1289  
1290  
1291  
1292  
1293  
1294  
1295  
1296  
1297  
1298  
1299  
1300  
1301  
1302  
1303  
1304  
1305  
1306  
1307  
1308  
1309  
1310  
1311  
1312  
1313  
1314  
1315  
1316  
1317  
1318  
1319  
1320  
1321  
1322  
1323  
1324  
1325  
1326  
1327  
1328  
1329  
1330  
1331  
1332  
1333  
1334  
1335  
1336  
1337  
1338  
1339  
1340  
1341  
1342  
1343  
1344  
1345  
1346  
1347  
1348  
1349  
1350  
1351  
1352  
1353  
1354  
1355  
1356  
1357  
1358  
1359  
1360  
1361  
1362  
1363  
1364  
1365  
1366  
1367  
1368  
1369  
1370  
1371  
1372  
1373  
1374  
1375  
1376  
1377  
1378  
1379  
1380  
1381  
1382  
1383  
1384  
1385  
1386  
1387  
1388  
1389  
1390  
1391  
1392  
1393  
1394  
1395  
1396  
1397  
1398  
1399  
1400  
1401  
1402  
1403  
1404  
1405  
1406  
1407  
1408  
1409  
1410  
1411  
1412  
1413  
1414  
1415  
1416  
1417  
1418  
1419  
1420  
1421  
1422  
1423  
1424  
1425  
1426  
1427  
1428  
1429  
1430  
1431  
1432  
1433  
1434  
1435  
1436  
1437  
1438  
1439  
1440  
1441  
1442  
1443  
1444  
1445  
1446  
1447  
1448  
1449  
1450  
1451  
1452  
1453  
1454  
1455  
1456  
1457  
1458  
1459  
1460  
1461  
1462  
1463  
1464  
1465  
1466  
1467  
1468  
1469  
1470  
1471  
1472  
1473  
1474  
1475  
1476  
1477  
1478  
1479  
1480  
1481  
1482  
1483  
1484  
1485  
1486  
1487  
1488  
1489  
1490  
1491  
1492  
1493  
1494  
1495  
1496  
1497  
1498  
1499  
1500  
1501  
1502  
1503  
1504  
1505  
1506  
1507  
1508  
1509  
1510  
1511  
1512  
1513  
1514  
1515  
1516  
1517  
1518  
1519  
1520  
1521  
1522  
1523  
1524  
1525  
1526  
1527  
1528  
1529  
1530  
1531  
1532  
1533  
1534  
1535  
1536  
1537  
1538  
1539  
1540  
1541  
1542  
1543  
1544  
1545  
1546  
1547  
1548  
1549  
1550  
1551  
1552  
1553  
1554  
1555  
1556  
1557  
1558  
1559  
1560  
1561  
1562  
1563  
1564  
1565  
1566  
1567  
1568  
1569  
1570  
1571  
1572  
1573  
1574  
1575  
1576  
1577  
1578  
1579  
1580  
1581  
1582  
1583  
1584  
1585  
1586  
1587  
1588  
1589  
1590  
1591  
1592  
1593  
1594  
1595  
1596  
1597  
1598  
1599  
1600  
1601  
1602  
1603  
1604  
1605  
1606  
1607  
1608  
1609  
1610  
1611  
1612  
1613  
1614  
1615  
1616  
1617  
1618  
1619  
1620  
1621  
1622  
1623  
1624  
1625  
1626  
1627  
1628  
1629  
1630  
1631  
1632  
1633  
1634  
1635  
1636  
1637  
1638  
1639  
1640  
1641  
1642  
1643  
1644  
1645  
1646  
1647  
1648  
1649  
1650  
1651  
1652  
1653  
1654  
1655  
1656  
1657  
1658  
1659  
1660  
1661  
1662  
1663  
1664  
1665  
1666  
1667  
1668  
1669  
1670  
1671  
1672  
1673  
1674  
1675  
1676  
1677  
1678  
1679  
1680  
1681  
1682  
1683  
1684  
1685  
1686  
1687  
1688  
1689  
1690  
1691  
1692  
1693  
1694  
1695  
1696  
1697  
1698  
1699  
1700  
1701  
1702  
1703  
1704  
1705  
1706  
1707  
1708  
1709  
1710  
1711  
1712  
1713  
1714  
1715  
1716  
1717  
1718  
1719  
1720  
1721  
1722  
1723  
1724  
1725  
1726  
1727  
1728  
1729  
1730  
1731  
1732  
1733  
1734  
1735  
1736  
1737  
1738  
1739  
1740  
1741  
1742  
1743  
1744  
1745  
1746  
1747  
1748  
1749  
1750  
1751  
1752  
1753  
1754  
1755  
1756  
1757  
1758  
1759  
1760  
1761  
1762  
1763  
1764  
1765  
1766  
1767  
1768  
1769  
1770  
1771  
1772  
1773  
1774  
1775  
1776  
1777  
1778  
1779  
1780  
1781  
1782  
1783  
1784  
1785  
1786  
1787  
1788  
1789  
1790  
1791  
1792  
1793  
1794  
1795  
1796  
1797  
1798  
1799  
1800  
1801  
1802  
1803  
1804  
1805  
1806  
1807  
1808  
1809  
1810  
1811  
1812  
1813  
1814  
1815  
1816  
1817  
1818  
1819  
1820  
1821  
1822  
1823  
1824  
1825  
1826  
1827  
1828  
1829  
1830  
1831  
1832  
1833  
1834  
1835  
1836  
1837  
1838  
1839  
1840  
1841  
1842  
1843  
1844  
1845  
1846  
1847  
1848  
1849  
1850  
1851  
1852  
1853  
1854  
1855  
1856  
1857  
1858  
1859  
1860  
1861  
1862  
1863  
1864  
1865  
1866  
1867  
1868  
1869  
1870  
1871  
1872  
1873  
1874  
1875  
1876  
1877  
1878  
1879  
1880  
1881  
1882  
1883  
1884  
1885  
1886  
1887  
1888  
1889  
1890  
1891  
1892  
1893  
1894  
1895  
1896  
1897  
1898  
1899  
1900  
1901  
1902  
1903  
1904  
1905  
1906  
1907  
1908  
1909  
1910  
1911  
1912  
1913  
1914  
1915  
1916  
1917  
1918  
1919  
1920  
1921  
1922  
1923  
1924  
1925  
1926  
1927  
1928  
1929  
1930  
1931  
1932  
1933  
1934  
1935  
1936  
1937  
1938  
1939  
1940  
1941  
1942  
1943  
1944  
1945  
1946  
1947  
1948  
1949  
1950  
1951  
1952  
1953  
1954  
1955  
1956  
1957  
1958  
1959  
1960  
1961  
1962  
1963  
1964  
1965  
1966  
1967  
1968  
1969  
1970  
1971  
1972  
1973  
1974  
1975  
1976  
1977  
1978  
1979  
1980  
1981  
1982  
1983  
1984  
1985  
1986  
1987  
1988  
1989  
1990  
1991  
1992  
1993  
1994  
1995  
1996  
1997  
1998  
1999  
2000  
2001  
2002  
2003  
2004  
2005  
2006  
2007  
2008  
2009  
2010  
2011  
2012  
2013  
2014  
2015  
2016  
2017  
2018  
2019  
2020  
2021  
2022  
2023  
2024  
2025  
2026  
2027  
2028  
2029  
2030  
2031  
2032  
2033  
2034  
2035  
2036  
2037  
2038  
2039  
2040  
2041  
2042  
2043  
2044  
2045  
2046  
2047  
2048  
2049  
2050  
2051  
2052  
2053  
2054  
2055  
2056  
2057  
2058  
2059  
2060  
2061  
2062  
2063  
2064  
2065  
2066  
2067  
2068  
2069  
2070  
2071  
2072  
2073  
2074  
2075  
2076  
2077  
2078  
2079  
2080  
2081  
2082  
2083  
2084  
2085  
2086  
2087  
2088  
2089  
2090  
2091  
2092  
2093  
2094  
2095  
2096  
2097  
2098  
2099  
2100  
2101  
2102  
2103  
2104  
2105  
2106  
2107  
2108  
2109  
2110  
2111  
2112  
2113  
2114  
2115  
2116  
2117  
2118  
2119  
2120  
2121  
2122  
2123  
2124  
2125  
2126  
2127  
2128  
2129  
2130  
2131  
2132  
2133  
2134  
2135  
2136  
2137  
2138  
2139  
2140  
2141  
2142  
2143  
2144  
2145  
2146  
2147  
2148  
2149  
2150  
2151  
2152  
2153  
2154  
2155  
2156  
2157  
2158  
2159  
2160  
2161  
2162  
2163  
2164  
2165  
2166  
2167  
2168  
2169  
2170  
2171  
2172  
2173  
2174  
2175  
2176  
2177  
2178  
2179  
2180  
2181  
2182  
2183  
2184  
2185  
2186  
2187  
2188  
2189  
2190  
2191  
2192  
2193  
2194  
2195  
2196  
2197  
2198  
2199  
2200  
2201  
220

1 14. The method of claim 9 wherein said determining the occurrence  
2 of a predetermined error event pattern in said recovered data  
3 output signal comprises determining the occurrence of  $ex = \pm\{1\}$  in  
4 said recovered data output signal.

1 15. The method of claim 9 wherein said determining the occurrence  
2 of a predetermined error event pattern in said recovered data  
3 output signal comprises determining the occurrence of  $ex = \pm\{1-11\}$   
4 in said recovered data output signal.

1 16. The method of claim 9 wherein said determining the occurrence  
2 of a predetermined error event pattern in said recovered data  
3 output signal comprises determining the occurrence of  $ex = \pm\{1-1\}$   
4 in said recovered data output signal.

1 17. The method of claim 9 wherein said determining the occurrence  
2 of a predetermined error event pattern in said recovered data  
3 output signal comprises determining a data sequence having a high  
4 likelihood of occurrence.

1 18. A post-processor circuit for use in a sampled data read channel  
2 of a mass data storage device, comprising:

3 a Viterbi detector that receives an actual sampled partial  
4 response target signal from a storage medium of said mass data  
5 storage device to produce a recovered data output signal;

6 an error pattern detector to generate an error pattern event  
7 indicating signal if a predetermined error event pattern occurs in  
8 said sampled partial response target signal;

9 a circuit for generating an error signal based upon a  
10 difference between said recovered data output signal and a delayed  
11 said actual sampled partial response target signal;

12 a threshold circuit to generate an error correction control  
13 signal if a magnitude of said error signal exceeds a predetermined  
14 threshold;

15 and an error correction circuit to modify the recovered data  
16 output signal when said error correction control signal and said  
17 error event pattern indicating occurrence signal are generated.

1 19. The circuit of claim 18 further comprising a whitening filter  
2 connected to receive said error signal to produce an input signal  
3 to said threshold circuit.

1 20. The circuit of claim 19 wherein said whitening filter has a  
2 transfer function,  $NW(D)$ , that is equal to

3 
$$(1+a_1D+a_2D^2+\dots+a_nD^n)/(1+b_1D+b_2D^2+\dots+b_mD^m),$$

4 in which  $a_1, a_2, \dots, a_n$ , and  $b_1, b_2, \dots, b_m$  are  
5 coefficients related to a density in which data is recorded in said  
6 mass data storage device.

1 21. The circuit of claim 19 wherein said whitening filter has a  
2 transfer function,  $NW(D)$ , that is equal to

3 
$$(1+a_1D+a_2D^2+a_3D^3)/(1+D),$$

4 in which  $a_1, a_2$ , and  $a_3$  are coefficients related to a density in  
5 which data is recorded in said mass data storage device.

1 22. The circuit of claim 18 wherein said predetermined error  
2 pattern event is  $ex = \pm\{1\}$ .

1 23. The circuit of claim 18 wherein said predetermined error  
2 pattern event is  $ex = \pm\{1-11\}$ .

1 24. The circuit of claim 18 wherein said predetermined error  
2 pattern event is  $ex = \pm\{1-1\}$ .

1 25. The circuit of claim 18 wherein said circuit for generating an  
2 error signal is an FIR filter

1 26. The circuit of claim 18 wherein said circuit for generating an  
2 error signal is an error pattern matched filter.

1 27. The circuit of claim 18 wherein said circuit for generating an  
2 error signal comprises a whitening noise generator and an FIR  
3 filter connected to receive an output of said whitening noise  
4 generator.

1 28. The circuit of claim 18 wherein said Viterbi detector has a  
2 partial response level of at least  $EPR4$ .

1 29. The circuit of claim 18 wherein said Viterbi detector has a  
2 partial response level of at least  $EEPR4$ .

# ABSTRACT OF THE DISCLOSURE

A post-processor (10) is added to a PRML read channel in a mass data storage device for improving the error rate performance. The post-processor (10) includes dominant error pattern detection  
5 filters, which include a noise-whitening filter (32) and an error pattern matched filter (34). The post-processor improves performance by whitening the colored noise which bring the noise correlation loss, and by generating an error signal when one of the dominant error patterns is detected to enable the data output to be  
10 properly corrected.



200

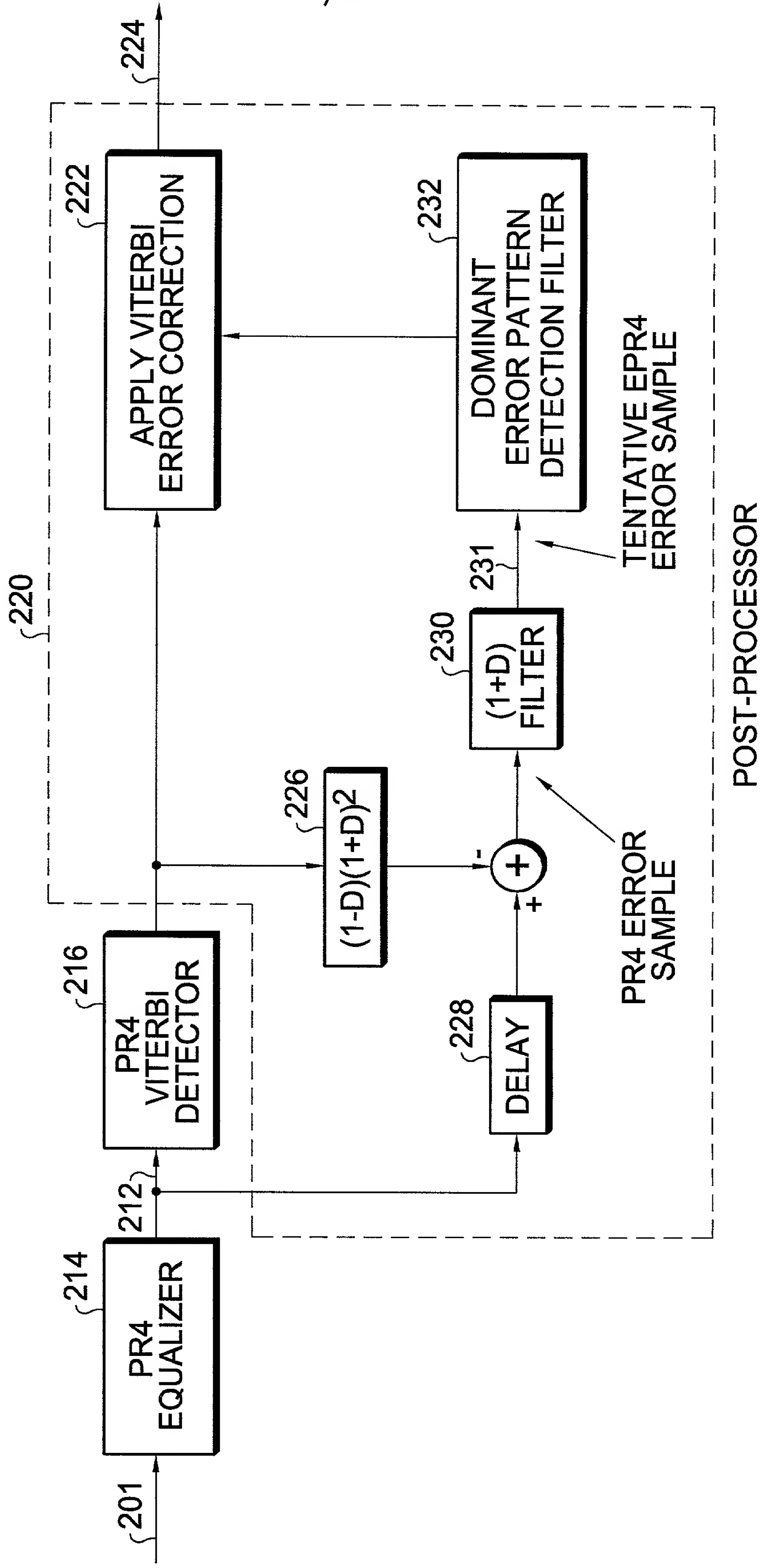


FIG. 1  
PRIOR ART

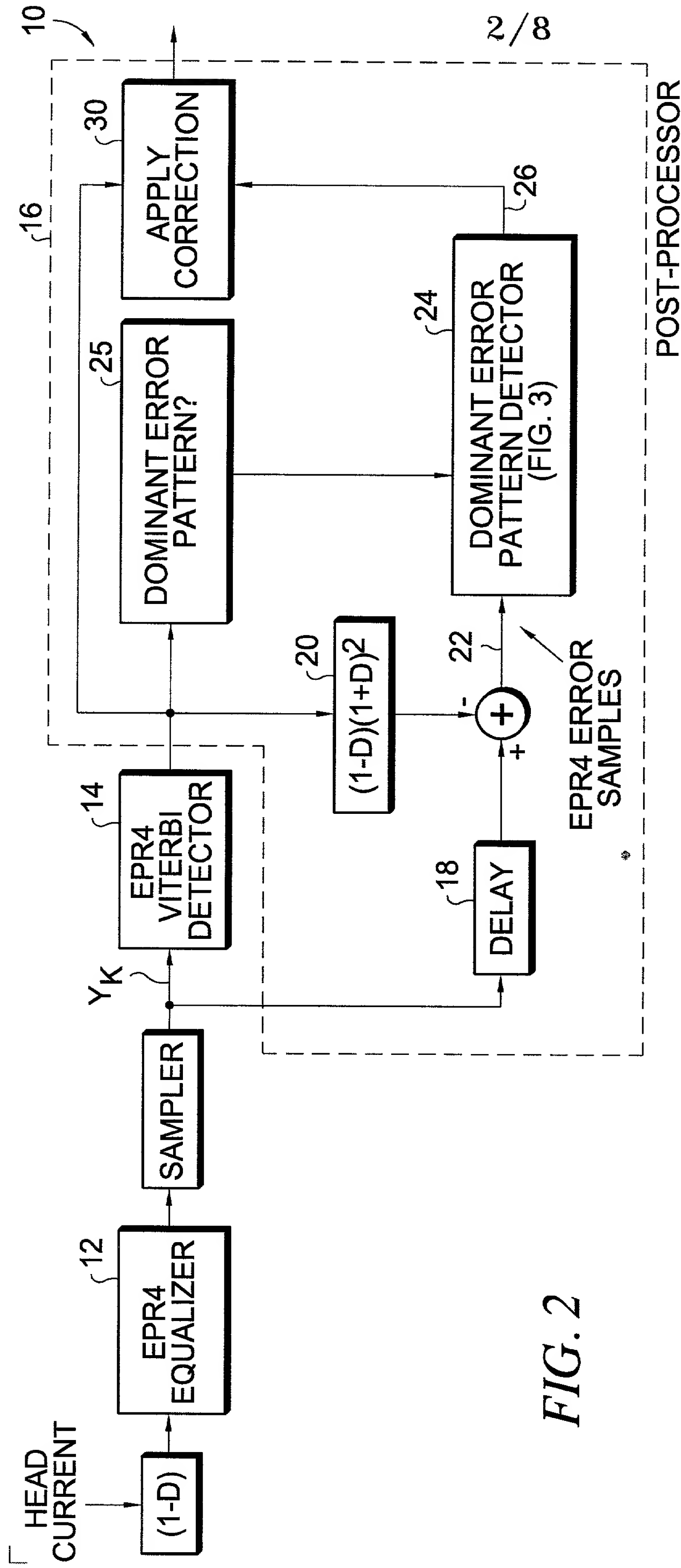


FIG. 2

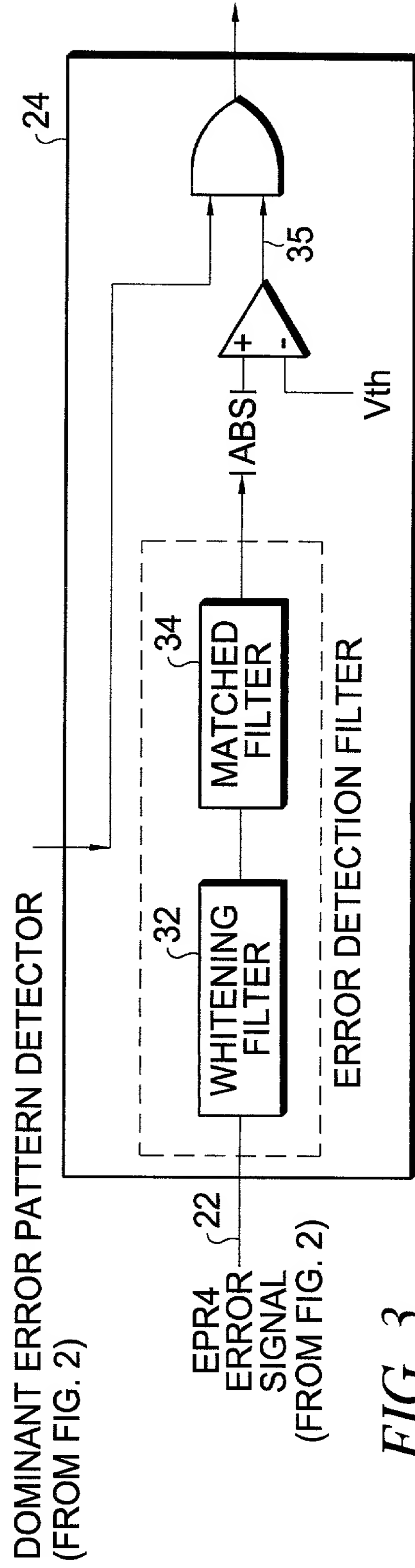


FIG. 3

Contact:  
Groover & Bachand  
5353 Wyoming Blvd., NE, Suite 3  
Albuquerque, New Mexico 87109-3132  
Tel: (505)823-1993

Re formal drawings for patent application:

Applicant: Ryohei Kuki

Application No:

Filed: Herewith

Title: POST-PROCESSOR USING A NOISE  
WHITENED MATCHED FILTER FOR A MASS DATA  
STORAGE DEVICE, OR THE LIKE

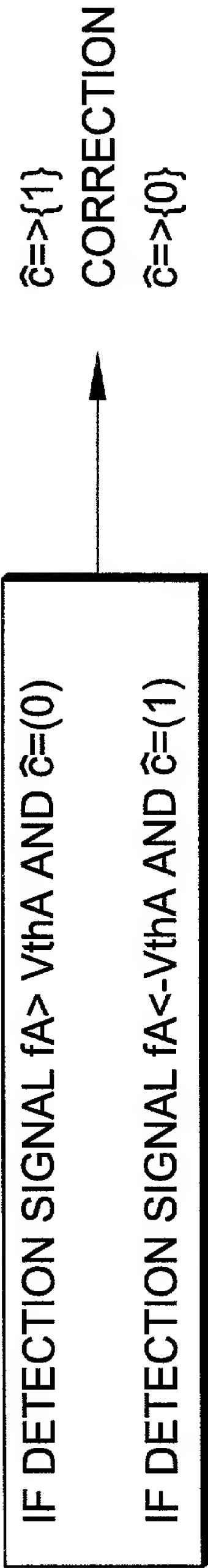
Docket no: TI-28532

Page 3/8

---

02 05 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000 1001 1002 1003 1004 1005 1006 1007 1008 1009 1010 1011 1012 1013 1014 1015 1016 1017 1018 1019 1020 1021 1022 1023 1024 1025 1026 1027 1028 1029 1030 1031 1032 1033 1034 1035 1036 1037 1038 1039 1040 1041 1042 1043 1044 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1061 1062 1063 1064 1065 1066 1067 1068 1069 1070 1071 1072 1073 1074 1075 1076 1077 1078 1079 1080 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110 1111 1112 1113 1114 1115 1116 1117 1118 1119 1120 1121 1122 1123 1124 1125 1126 1127 1128 1129 1130 1131 1132 1133 1134 1135 1136 1137 1138 1139 1140 1141 1142 1143 1144 1145 1146 1147 1148 1149 1150 1151 1152 1153 1154 1155 1156 1157 1158 1159 1160 1161 1162 1163 1164 1165 1166 1167 1168 1169 1170 1171 1172 1173 1174 1175 1176 1177 1178 1179 1180 1181 1182 1183 1184 1185 1186 1187 1188 1189 1190 1191 1192 1193 1194 1195 1196 1197 1198 1199 1200 1201 1202 1203 1204 1205 1206 1207 1208 1209 1210 1211 1212 1213 1214 1215 1216 1217 1218 1219 1220 1221 1222 1223 1224 1225 1226 1227 1228 1229 1230 1231 1232 1233 1234 1235 1236 1237 1238 1239 1240 1241 1242 1243 1244 1245 1246 1247 1248 1249 1250 1251 1252 1253 1254 1255 1256 1257 1258 1259 1260 1261 1262 1263 1264 1265 1266 1267 1268 1269 1270 1271 1272 1273 1274 1275 1276 1277 1278 1279 1280 1281 1282 1283 1284 1285 1286 1287 1288 1289 1290 1291 1292 1293 1294 1295 1296 1297 1298 1299 1300 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310 1311 1312 1313 1314 1315 1316 1317 1318 1319 1320 1321 1322 1323 1324 1325 1326 1327 1328 1329 1330 1331 1332 1333 1334 1335 1336 1337 1338 1339 1340 1341 1342 1343 1344 1345 1346 1347 1348 1349 1350 1351 1352 1353 1354 1355 1356 1357 1358 1359 1360 1361 1362 1363 1364 1365 1366 1367 1368 1369 1370 1371 1372 1373 1374 1375 1376 1377 1378 1379 1380 1381 1382 1383 1384 1385 1386 1387 1388 1389 1390 1391 1392 1393 1394 1395 1396 1397 1398 1399 1400 1401 1402 1403 1404 1405 1406 1407 1408 1409 1410 1411 1412 1413 1414 1415 1416 1417 1418 1419 1420 1421 1422 1423 1424 1425 1426 1427 1428 1429 1430 1431 1432 1433 1434 1435 1436 1437 1438 1439 1440 1441 1442 1443 1444 1445 1446 1447 1448 1449 1450 1451 1452 1453 1454 1455 1456 1457 1458 1459 1460 1461 1462 1463 1464 1465 1466 1467 1468 1469 1470 1471 1472 1473 1474 1475 1476 1477 1478 1479 1480 1481 1482 1483 1484 1485 1486 1487 1488 1489 1490 1491 1492 1493 1494 1495 1496 1497 1498 1499 1500 1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513 1514 1515 1516 1517 1518 1519 1520 1521 1522 1523 1524 1525 1526 1527 1528 1529 1530 1531 1532 1533 1534 1535 1536 1537 1538 1539 1540 1541 1542 1543 1544 1545 1546 1547 1548 1549 1550 1551 1552 1553 1554 1555 1556 1557 1558 1559 1560 1561 1562 1563 1564 1565 1566 1567 1568 1569 1570 1571 1572 1573 1574 1575 1576 1577 1578 1579 1580 1581 1582 1583 1584 1585 1586 1587 1588 1589 1590 1591 1592 1593 1594 1595 1596 1597 1598 1599 1600 1601 1602 1603 1604 1605 1606 1607 1608 1609 1610 1611 1612 1613 1614 1615 1616 1617 1618 1619 1620 1621 1622 1623 1624 1625 1626 1627 1628 1629 1630 1631 1632 1633 1634 1635 1636 1637 1638 1639 1640 1641 1642 1643 1644 1645 1646 1647 1648 1649 1650 1651 1652 1653 1654 1655 1656 1657 1658 1659 1660 1661 1662 1663 1664 1665 1666 1667 1668 1669 1670 1671 1672 1673 1674 1675 1676 1677 1678 1679 1680 1681 1682 1683 1684 1685 1686 1687 1688 1689 1690 1691 1692 1693 1694 1695 1696 1697 1698 1699 1700 1701 1702 1703 1704 1705 1706 1707 1708 1709 1710 1711 1712 1713 1714 1715 1716 1717 1718 1719 1720 1721 1722 1723 1724 1725 1726 1727 1728 1729 1730 1731 1732 1733 1734 1735 1736 1737 1738 1739 1740 1741 1742 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752 1753 1754 1755 1756 1757 1758 1759 1760 1761 1762 1763 1764 1765 1766 1767 1768 1769 1770 1771 1772 1773 1774 1775 1776 1777 1778 1779 1780 1781 1782 1783 1784 1785 1786 1787 1788 1789 1790 1791 1792 1793 1794 1795 1796 1797 1798 1799 1800 1801 1802 1803 1804 1805 1806 1807 1808 1809 1810 1811 1812 1813 1814 1815 1816 1817 1818 1819 1820 1821 1822 1823 1824 1825 1826 1827 1828 1829 1830 1831 1832 1833 1834 1835 1836 1837 1838 1839 1840 1841 1842 1843 1844 1845 1846 1847 1848 1849 1850 1851 1852 1853 1854 1855 1856 1857 1858 1859 1860 1861 1862 1863 1864 1865 1866 1867 1868 1869 1870 1871 1872 1873 1874 1875 1876 1877 1878 1879 1880 1881 1882 1883 1884 1885 1886 1887 1888 1889 1890 1891 1892 1893 1894 1895 1896 1897 1898 1899 1900 1901 1902 1903 1904 1905 1906 1907 1908 1909 1910 1911 1912 1913 1914 1915 1916 1917 1918 1919 1920 1921 1922 1923 1924 1925 1926 1927 1928 1929 1930 1931 1932 1933 1934 1935 1936 1937 1938 1939 1940 1941 1942 1943 1944 1945 1946 1947 1948 1949 1950 1951 1952 1953 1954 1955 1956 1957 1958 1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975 1976 1977 1978 1979 1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100 2101 2102 2103 2104 2105 2106 2107 2108 2109 2110 2111 2112 2113 2114 2115 2116 2117 2118 2119 2120 2121 2122 2123 2124 2125 2126 2127 2128 2129 2130 2131 2132 2133 2134 2135 2136 2137 2138 2139 2140 2141 2142 2143 2144 2145 2146 2147 2148 2149 2150 2151 2152 2153 2154 2155 2156 2157 2158 2159 2160 2161 2162 2163 2164 2165 2166 2167 2168 2169 2170 2171 2172 2173 2174 2175 2176 2177 2178 2179 2180 2181 2182 2183 2184 2185 2186 2187 2188 2189 2190 2191 2192 2193 2194 2195 2196 2197 2198 2199 2200 2201 2202 2203 2204 2205 2206 2207 2208 2209 2210 2211 2212 2213 2214 2215 2216 2217 2218 2219 2220 2221 2222 2223 2224 2225 2226 2227 2228 2229 2230 2231 2232 2233 2234 2235 2236 2237 2238 2239 2240 2241 2242 2243 2244 2245 2246 2247 2248 2249 2250 2251 2252 2253 2254 2255 2256 2257 2258 2259 2260 2261 2262 2263 2264 2265 2266 2267 2268 2269 2270 2271 2272 2273 2274 2275 2276 2277 2278 2279 2280 2281 2282 2283 2284 2285 2286 2287 2288 2289 2290 2291 2292 2293 2294 2295 2296 2297 2298 2299 2300 2301 2302 2303 2304 2305 2306 2307 2308 2309 2310 2311 2312 2313 2314 2315 2316 2317 2318 2319 2320 2321 2322 2323 2324 2325 2326 2327 2328 2329 2330 2331 2332 2333 2334 2335 2336 2337 2338 2339 2340 2341 2342 2343 2344 2345 2346 2347 2348 2349 2350 2351 2352 2353 2354 2355 2356 2357 2358 2359 2360 2361 2362 2363 2364 2365 2366 2367 2368 2369 2370 2371 2372 2373 2374 2375 2376 2377 2378 2379 2380 2381 2382 2383 2384 2385 2386 2387 2388 2389 2390 2391 2392 2393 2394 2395 2396 2397 2398 2399 2400 2401 2402 2403 2404 2405 2406 2407 2408 2409 2410 2411 2412 2413 2414 2415 2416 2417 2418 2419 2420 2421 2422 2423 2424 2425 2426 2427 2428 2429 2430 2431 2432 2433 2434 2435 2436 2437 2438 2439 2440 2441 2442 2443 2444 2445 2446 2447 2448 2449 2450 2451 2452 2453 2454 2455 2456 2457 2458 2459 2460 2461 2462 2463 2464 2465 2466 2467 2468 2469 2470 2471 2472 2473 2474 2475 2476 2477 2478 2479 2480 2481 2482 2483 2484 2485 2486 2487 2488 2489 2490 2491 2492 2493 2494 2495 2496 2497 2498 2499 2500 2501 2502 2503 2504 2505 2506 2507 2508 2509 2510 2511 2512 2513 2514 2515 2516 2517 2518 2519 2520 2521 2522 2523 2524 2525 2526 2527 2528 2529 2530 2531 2532 2533 2534 2535 2536 2537 2538 2539 2540 2541 2542 2543 2544 2545 2546 2547 2548 2549 2550 2551 2552 2553 2554 2555 2556 2557 2558 2559 2560 2561 2562 2563 2564 2565 2566 2567 2568 2569 2570 2571 2572 2573 2574 2575 2576 2577 2578 2579 2580 2581 2582 2583 2584 2585 2586 2587 2588 2589 2590 2591 2592 2593 2594 2595 2596 2597 2598 2599 2600 2601 2602 2603 2604 2605 2606 2607 2608 2609 2610 2611 2612 2613 2614 2615 2616

ERROR EVENT A (ex={1} OR ex={-1})



ERROR EVENT B (ex={1,-1,1} OR ex={-1,1,-1})

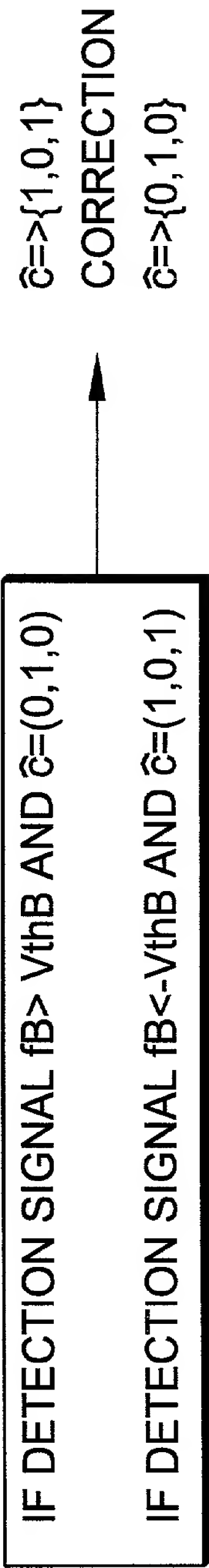


FIG. 5

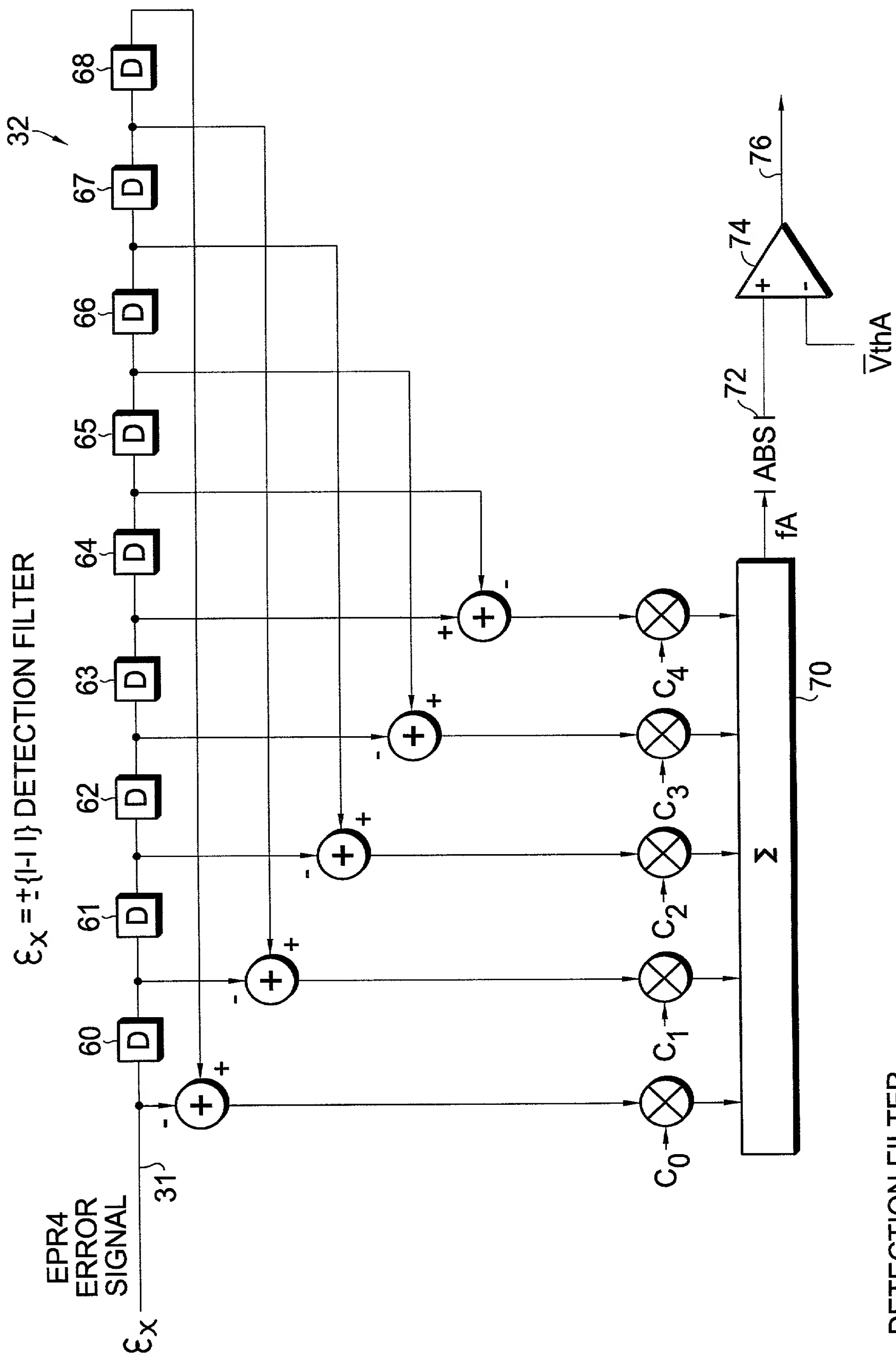
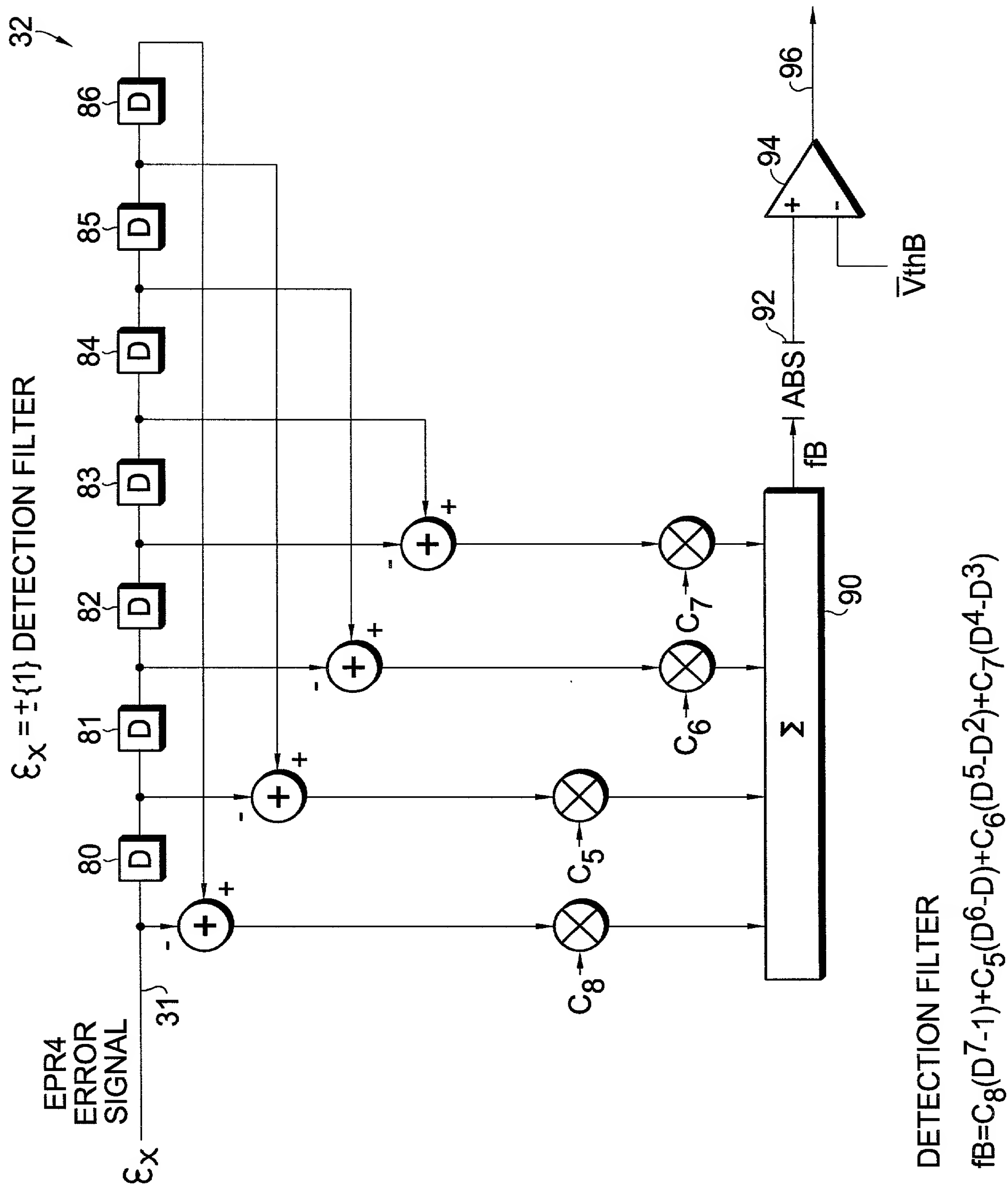


FIG. 6

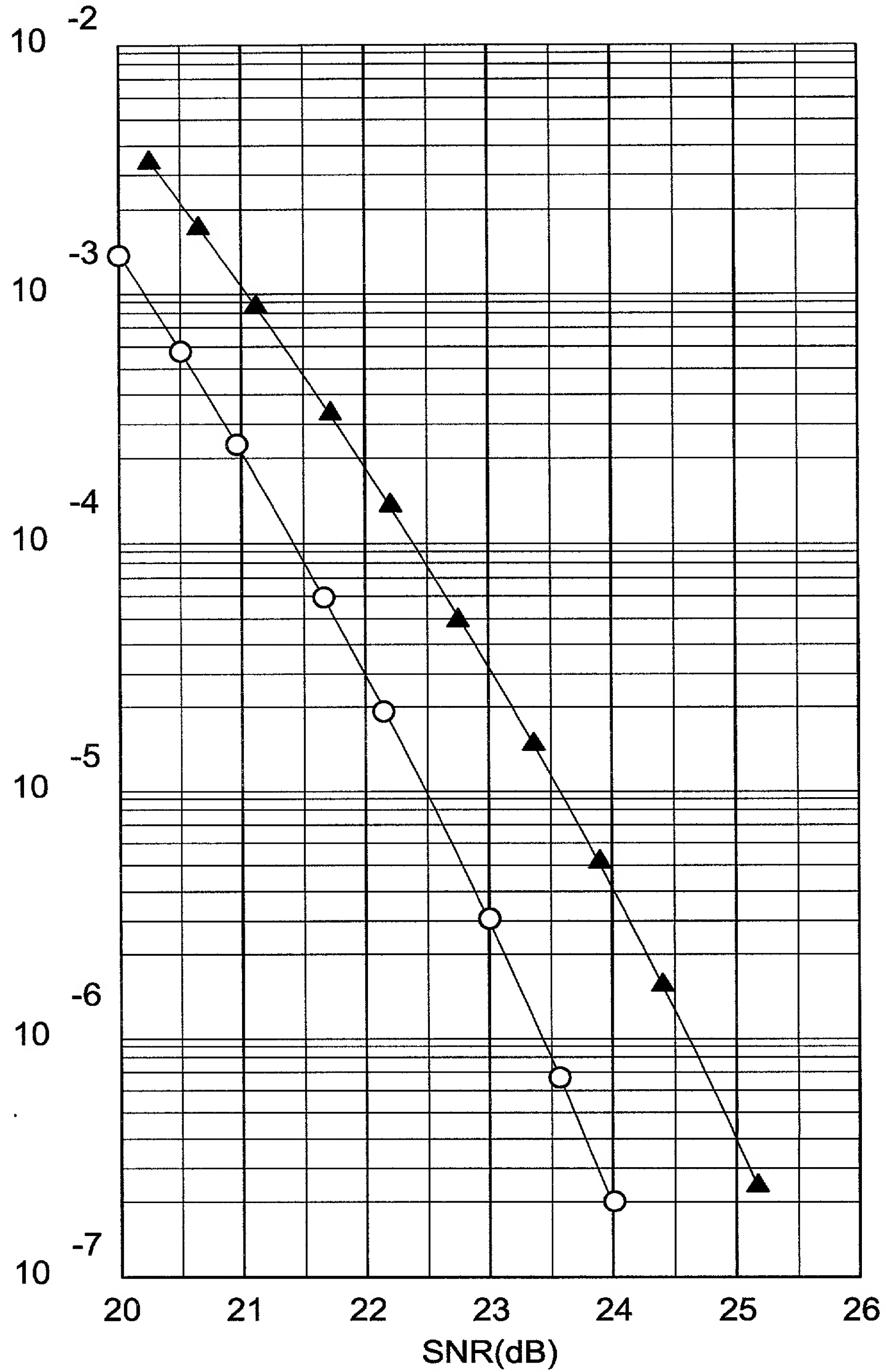


**FIG. 7**



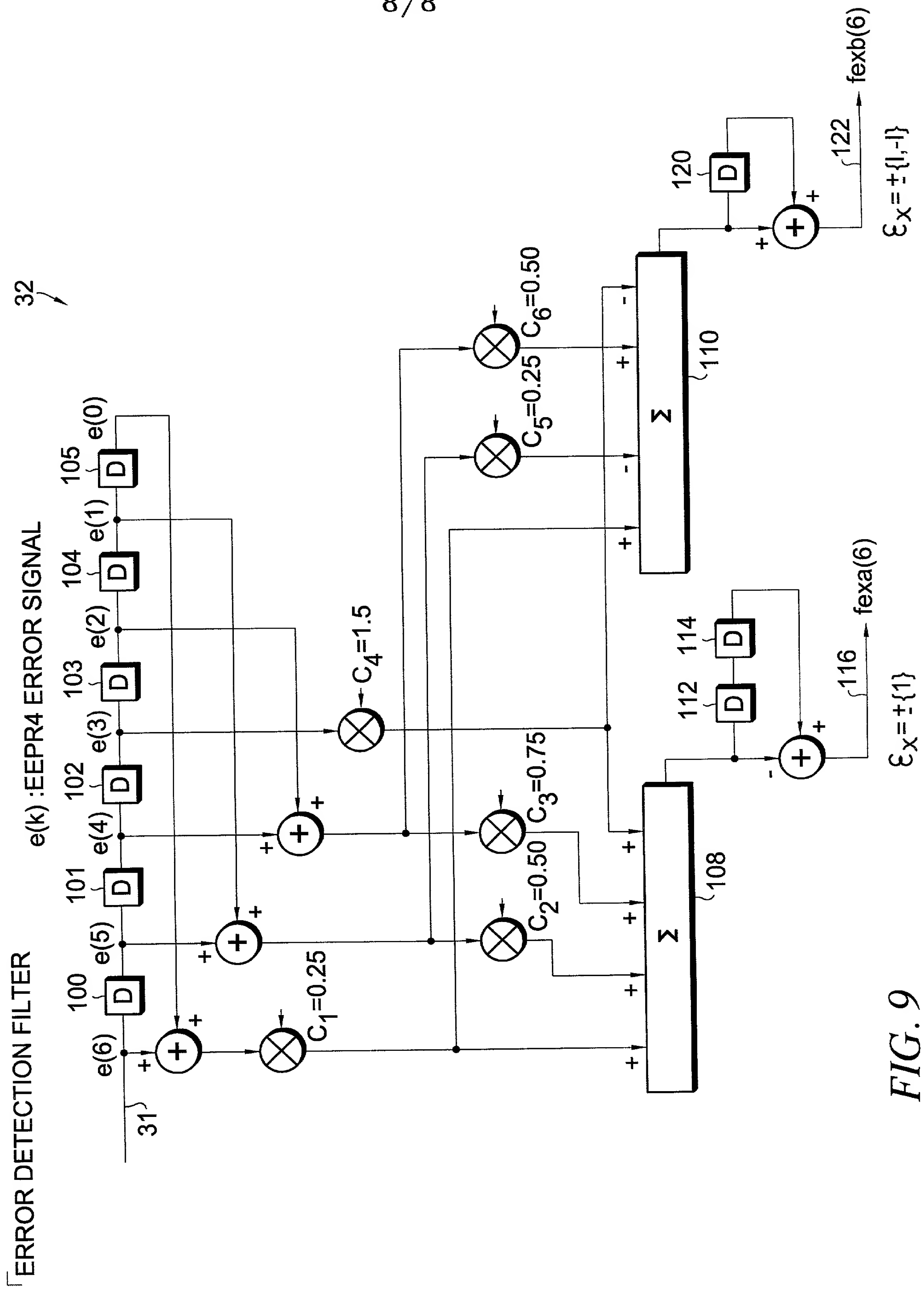
## BIT ERROR RATE VS SNR

BIT ERROR RATE



▲ W/O POST PROCESSOR  
○ WITH POST PROCESSOR

*FIG. 8*



# APPLICATION FOR UNITED STATES PATENT

## DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor of plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:  
POST-PROCESSOR USING A NOISE WHITENED MATCHED FILTER FOR A MASS DATA STORAGE  
DEVICE, OR THE LIKE

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS/AGENTS TO PROSECUTE  
THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND  
TRADEMARK OFFICE CONNECTED THEREWITH

Richard L. Donaldson, Reg. No. 25,673, W. Daniel Swayze, Jr., Reg. No. 34,478, Jay M. Cantor, Reg.  
No. 19,906, W. James Brady III, Reg. No. 32,080, Robby T. Holland, Reg. No. 33,304, Alan K. Steward,  
Reg. No. 35,373, Christopher L. Maginniss, Reg. No. 30,288, Mark E. Courtney, Agent, Reg. No. 36,491.

SEND CORRESPONDENCE TO:  
Texas Instruments Incorporated  
P. O. Box 655474, M/S 3999  
Dallas, TX 75265

DIRECT TELEPHONE CALLS TO:  
W. Daniel Swayze, Jr.  
(972) 917-5633

NAME OF INVENTOR: (1)  
Ryohei Kuki

NAME OF INVENTOR (2)  
Koshiro Saeki

NAME OF INVENTOR (3)

RESIDENCE (City & State Only)  
Tokyo, Japan

RESIDENCE (City & State Only)  
Irvine, California

RESIDENCE (City & State Only)

Post Office Address  
5-29-41-201 Tayosho,  
Tokyo, Koto-ku, 135-0016

Post Office Address  
23, Snowapple  
Irvine, Orange, California 92614

Post Office Address

COUNTRY OF CITIZENSHIP:  
Japan

COUNTRY OF CITIZENSHIP:  
Japan

COUNTRY OF CITIZENSHIP:

SIGNATURE OF INVENTOR:

SIGNATURE OF INVENTOR:

SIGNATURE OF INVENTOR:

DATE:

DATE:

DATE: